ABSTRACT OF THE DISCLOSURE

The operating characteristic of a transistor, modeled by a resistive element having fixed resistance and a power source voltage that varies with time, is segmented into a linearity region in which a current increases as a gate potential varies and a saturation region in which the current gradually decreases as the gate potential remains at a constant level, so that gradual decrease in current in a saturation region of the transistor is properly reflected and a delay time is estimated in a precise manner.